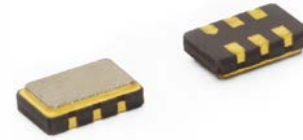


# Model 633

## Very Low Jitter LVPECL or LVDS Clock

### Features

- Ceramic Surface Mount Package
- Very Low Phase Jitter Performance, 500fs Maximum
- Fundamental or 3<sup>rd</sup> Overtone Crystal Design
- Frequency Range 10 – 220MHz \*
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418



Part Dimensions:  
3.2 × 2.5 × 1.0mm • 25.00mg

### Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

#### Standard Frequencies

- 50.00MHz
- 125.00MHz
- 148.3516MHz
- 200.0000MHz
- 155.52MHz
- 156.25MHz
- 161.1328MHz

\* Check with factory for availability.

### Description

CTS Model 633 is a low cost, high performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M633 has excellent stability and very low jitter/phase noise performance.

### Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging
633	P	XXX or XXXX	3	I	3	T

Code	Output
P	LVPECL - Pin 1 Enable
L	LVDS - Pin 1 Enable
E	LVPECL - Pin 2 Enable
V	LVDS - Pin 2 Enable

Code	Stability
6	±20ppm <sup>2</sup>
5	±25ppm
3	±50ppm
2	±100ppm

Code	Voltage
2	+2.5Vdc
3	+3.3Vdc

Code	Temp. Range
A	-10°C to +60°C
C	-20°C to +70°C
I	-40°C to +85°C

Code	Frequency
	Product Frequency Code <sup>1</sup>

Code	Packing
T	1k pcs./reel

Notes:

- 1] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2] Consult factory for availability of 6I Stability/Temperature combination.

**Not all performance combinations and frequencies may be available.**  
**Contact your local CTS Representative or CTS Customer Service for availability.**

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.

## Electrical Specifications

## Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	$V_{CC}$	-	-0.5	-	5.0	V
Supply Voltage	$V_{CC}$	±5%	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current						
LVPECL	$I_{CC}$	Maximum Load	-	55	88	mA
LVDS			-	45	66	
Operating Temperature	$T_A$	-	-20 -40	+25	+70 +85	°C
Storage Temperature	$T_{STG}$	-	-40	-	+125	°C

## Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range						
LVPECL	$f_0$	-		10 - 220		MHz
LVDS				10 - 220		
Frequency Stability [Note 1]	$\Delta f/f_0$	-		20, 25, 50 or 100		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal $V_{CC}$	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

## Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	$R_L$	Terminated to $V_{CC} - 2.0V$	-	50	-	Ohms
Output Voltage Levels	$V_{OH}$	PECL Load, -20°C to +70°C	$V_{CC} - 1.025$	-	$V_{CC} - 0.880$	V
	$V_{OL}$		$V_{CC} - 1.810$	-	$V_{CC} - 1.620$	
	$V_{OH}$	PECL Load, -40°C to +85°C	$V_{CC} - 1.085$	-	$V_{CC} - 0.880$	V
	$V_{OL}$		$V_{CC} - 1.830$	-	$V_{CC} - 1.555$	
Output Duty Cycle	SYM	@ $V_{CC} - 1.3V$	45	-	55	%
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $R_L = 50$ Ohms	-	0.3	0.7	ns
Output Type	-	-		LVDS		-
Output Load	$R_L$	Between Outputs	-	100	-	Ohms
Output Voltage Levels	$V_{OH}$	LVDS Load	-	1.43	1.60	V
	$V_{OL}$		0.90	1.10	-	
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	$V_{OD}$	$R_L = 100$ Ohms	247	330	454	mV
Offset Voltage	$V_{OS}$	LVDS Load	1.125	1.25	1.375	V
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $R_L = 100$ Ohms	-	0.4	0.7	ns

### Electrical Specifications

#### Output Parameters

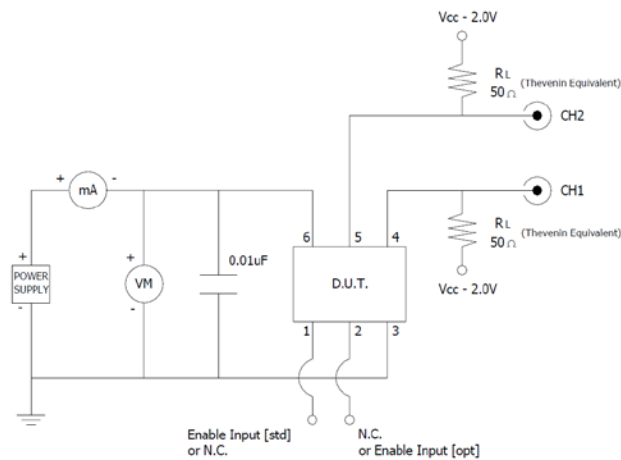
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	$T_S$	Application of $V_{CC}$	-	2	5	ms
<b>Enable Function [Standby]</b>						
Enable Input Voltage	$V_{IH}$	Pin 1 or 2 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	$V_{IL}$	Pin 1 or 2 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Disable Time	$T_{PLZ}$	Pin 1 or 2 Logic '0', Output Disabled	-	-	200	ns
Enable Time	$T_{PLZ}$	Pin 1 or 2 Logic '1', Output Enabled	-	-	2	ms
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	300	500	fs
Period Jitter, RMS	pjrms	-	-	2.6	-	ps
Period Jitter, pk-pk	pjpk-pk	-	-	25	-	ps

#### Enable Truth Table

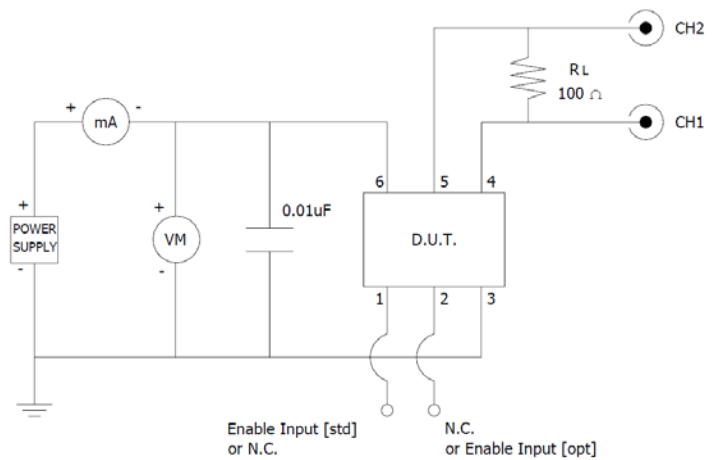
Pin 1 or Pin 2	Pin 4 & Pin 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

#### Test Circuit

LVPECL

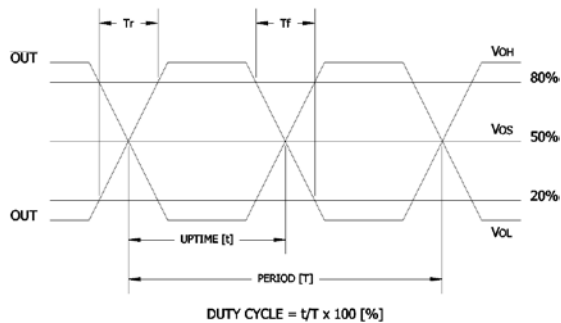


LVDS



#### Output Waveform

LVPECL or LVDS

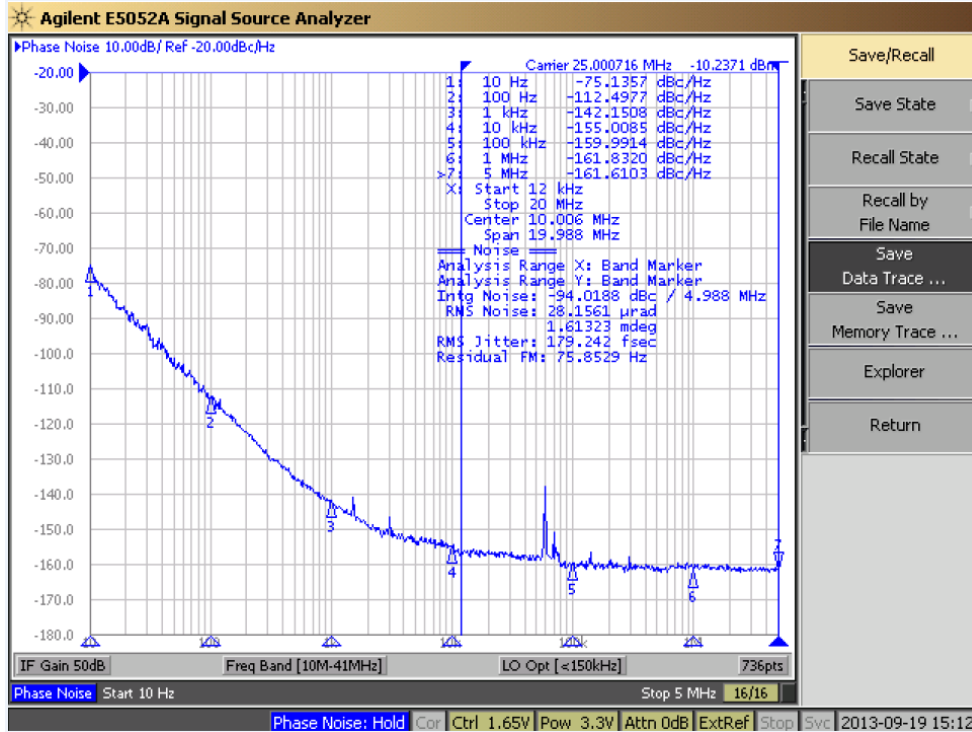


## Electrical Specifications

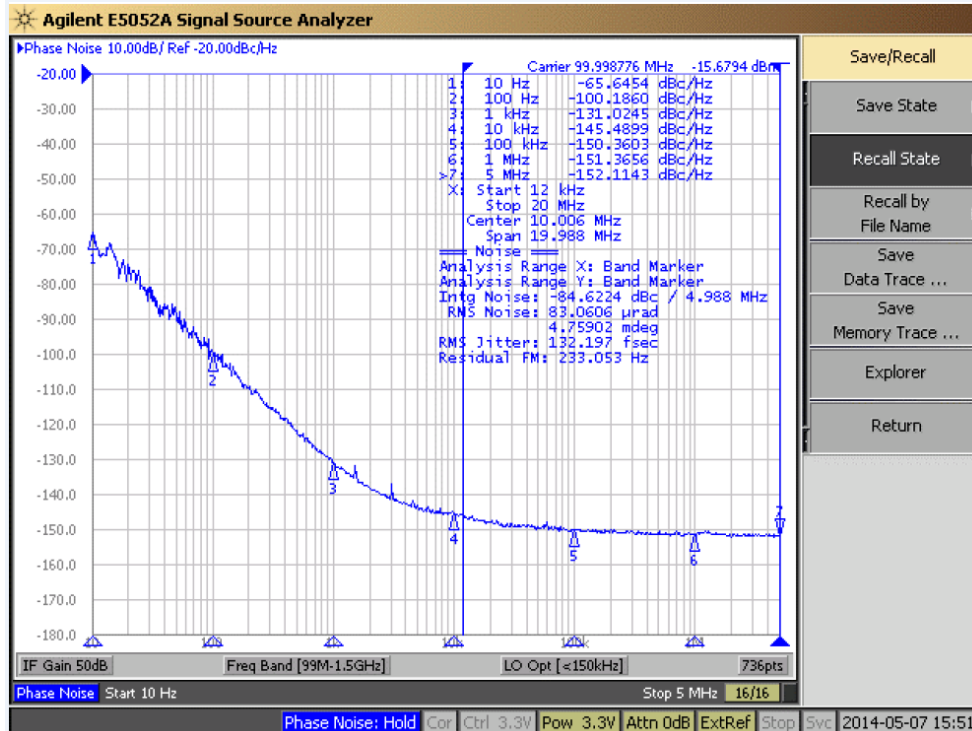
### Performance Data

Phase Noise [typical]

25MHz, LVPECL,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$



100MHz, LVPECL,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$

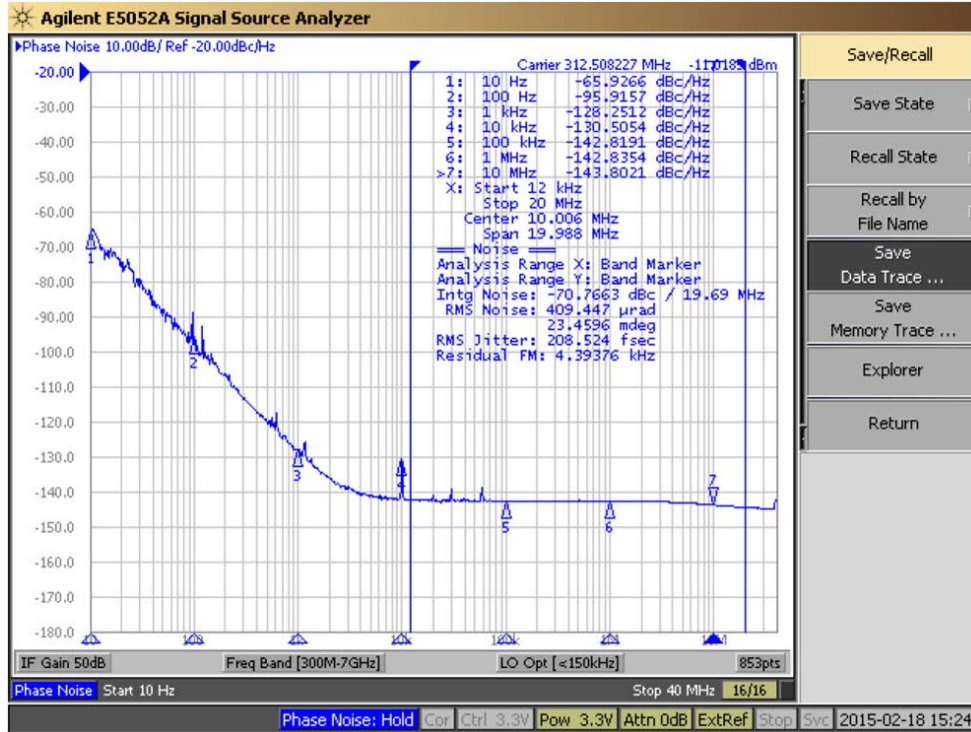


## Electrical Specifications

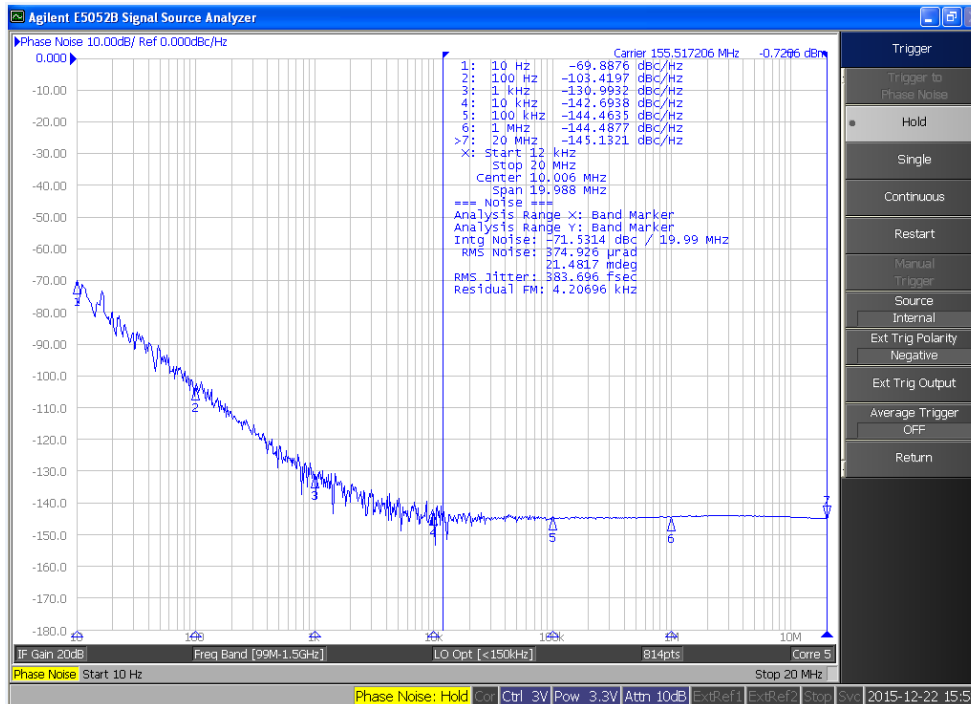
### Performance Data

#### Phase Noise [typical]

312.50MHz, LVPECL,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$



155.52MHz, LVDS,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$



## Electrical Specifications

### Phase Noise Tabulated

Typical,  $V_{CC} = 3.3V$ ,  $T_A = +25^{\circ}C$

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVPECL @ 25.00MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-75.14	
		@ 100Hz	-112.50	
		@ 1kHz	-142.15	dBc/Hz
		@ 10kHz	-155.01	
		@ 100kHz	-159.99	
		@ 1MHz	-161.83	
	@ 5MHz	-161.61		
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	179.24	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVPECL @ 312.20MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-65.93	
		@ 100Hz	-95.92	
		@ 1kHz	-128.25	dBc/Hz
		@ 10kHz	-130.51	
		@ 100kHz	-142.82	
		@ 1MHz	-142.84	
	@ 10MHz	-143.80		
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	208.52	fs

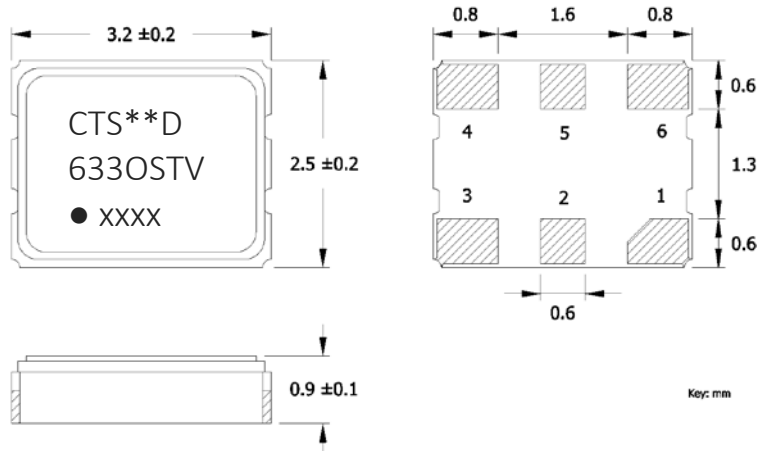
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVPECL @ 100.00MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-65.65	
		@ 100Hz	-100.19	
		@ 1kHz	-131.02	dBc/Hz
		@ 10kHz	-145.49	
		@ 100kHz	-150.36	
		@ 1MHz	-151.37	
	@ 5MHz	-152.11		
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	132.20	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVDS @ 155.52MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-69.89	
		@ 100Hz	-103.42	
		@ 1kHz	-130.99	dBc/Hz
		@ 10kHz	-142.69	
		@ 100kHz	-144.46	
		@ 1MHz	-144.49	
	@ 20MHz	-145.13		
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	383.70	fs

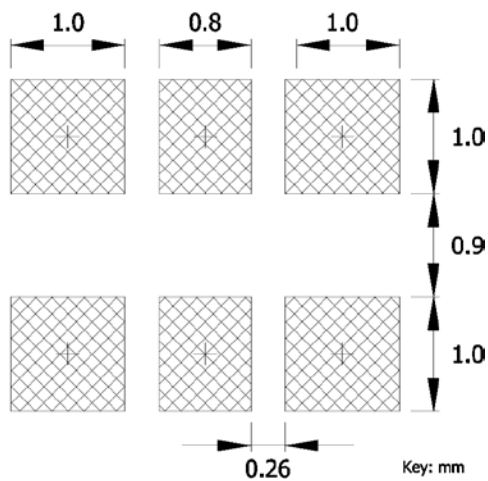


### Mechanical Specifications

#### Package Drawing



#### Recommended Pad Layout



#### Pin Assignments

Pin	Symbol	Function
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	$V_{CC}$	Supply Voltage

Table I - Date Code

		MONTH					YEAR														
		JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC								
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M					
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z					
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m					
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z					

#### Marking Information

##### Option 1 [3 lines, 7 characters maximum per line]

- \*\* - Manufacturing Site Code.
  - D - Date Code. See Table I for codes.
  - O - Output Type; P or E = LVPECL, L or V = LVDS.
  - ST - Frequency Stability/Temperature Code. [Refer to Ordering Information]
  - V - Voltage Code; 3 = 3.3V, 2 = 2.5V.
  - xxxx - Frequency Code.  
3-digits, frequencies below 100MHz  
4-digits, frequencies 100MHz or greater
- [See document 016-1454-0, Frequency Code Tables.]

```
CTS**D
633OSTV
● xxxx
```

##### Option 2 [2 lines, 7 characters maximum per line]

- O - Output Type; P or E = LVPECL, L or V = LVDS.
  - ST - Frequency Stability/Temperature Code. [Refer to Ordering Information]
  - V - Voltage Code; 3 = 3.3V, 2 = 2.5V.
  - xxxx - Frequency Code.  
3-digits, frequencies below 100MHz  
4-digits, frequencies 100MHz or greater
- [See document 016-1454-0, Frequency Code Tables.]
- D - Date Code. See Table I for codes.
- [Note: Manufacturing site code must appear on reel and carton labels.]

```
633OSTV
● xxxxD
```

#### Notes

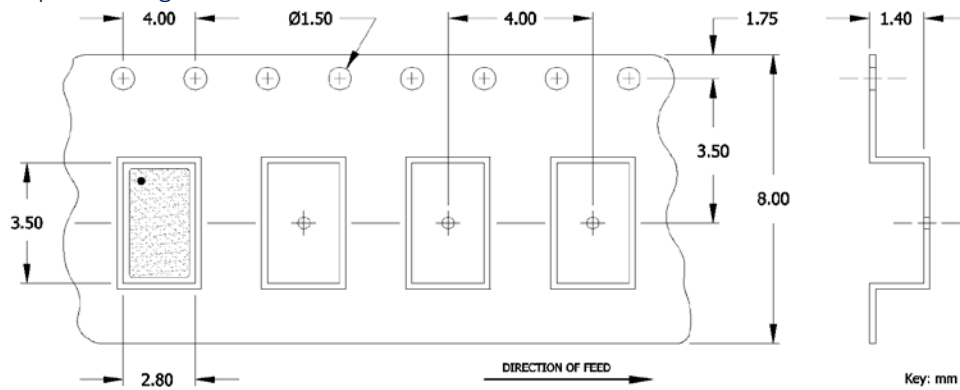
- JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- MSL = 1.

# Model 633

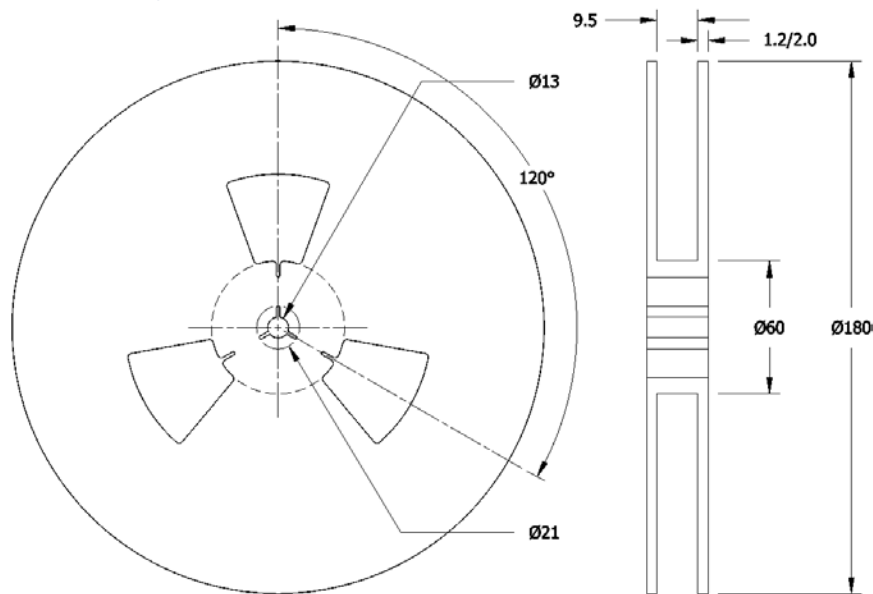
Very Low Jitter LVPECL or LVDS Clock

## Packaging - Tape and Reel

### Tape Drawing



### Reel Drawing



### Notes

1. Device quantity is 1k pieces minimum or 3k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.